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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/696,865	10/30/2003	Andreas C. Doering	RPS920030110US1	8071
47052	7590	07/28/2006	EXAMINER	
SAWYER LAW GROUP LLP			JOHNSON, BRIAN P	
PO BOX 51418			ART UNIT	
PALO ALTO, CA 94303			PAPER NUMBER	
			2183	

DATE MAILED: 07/28/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

**Office Action Summary**

Application No.

10/696,865

Applicant(s)

DOERING ET AL.

Examiner

Brian P. Johnson

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on May 22<sup>nd</sup>, 2006.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 1-18 and 20 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☒ Claim(s) 20 is/are allowed.
- 6) ☒ Claim(s) 1-18 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some \* c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
  2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

- |  |   |
|--|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892)   | 4) <input type="checkbox"/> Interview Summary (PTO-413)<br>Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)                                   | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152)             |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)<br>Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____  |

**DETAILED ACTION**

1. Claims 1-18 and 20 are pending.

***Papers Filed***

2. Examiner acknowledges receipt of amendments and remarks filed on May 22<sup>nd</sup>, 2006.

***Title***

3. Objection withdrawn.

***Allowable Subject Matter***

1. Claim 20 is allowed.

Regarding claim 20, the disclosed claim shows several additional limitations over previous claims. In particular, the additional limitation of multiple processors and multiple coprocessors was added; however, this limitation is considered to be obvious. A further non-obvious limitation of choosing a coprocessor unit based on a LRU algorithm (in essence, treating the processors like a cache) has also been added. For this reason, claim 20 is allowed over prior art.

***Claim Rejections - 35 USC § 102***

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

5. Claims 1-18 are rejected under 35 U.S.C. 102(e) as being anticipated by De Oliveira Kastrup Pereira et al. (U.S. Patent No. 6,721,884) hereinafter referred to as Pereira.

6. As per claim 1, Pereira discloses a method for dynamically programming a field programmable gate arrays (FPGA) in a coprocessor (Fig. 1 reconfigurable logic 18 and col. 1 lines 28-29), the coprocessor coupled to a processor (Fig. 1), the method comprising:

Providing a processor and a coprocessor (fig 1 reference 18) that is separate from the processor, the coprocessor being coupled to the processor and including a field programmable gate array (col 1 lines 28-29).

(a) executing an application using the processor; (Col. 4 lines 54-57)

(b) the coprocessor receiving an instruction from the processor to perform a function for the application; (Col. 5 lines 45-49)

(c) determining that the field programmable gate array (FPGA) in the coprocessor is not programmed to perform the function for the application; (Col. 5 lines 53-59)

(d) fetching a configuration bit stream associated with the function for the application responsive to the determination that the field programmable gate array (FPGA) is not programmed to perform the function for the application; (Col. 5 lines 53-59)

(e) dynamically programming the field programmable gate array (FPGA) in accordance with the configuration bit stream to perform the function for the application. (Col. 5 lines 53-59)

7. As per claim 2, Pereira discloses the method of claim 1, wherein the coprocessor further comprises:

an Auxiliary Processing Unit (APU) interface (Fig. 2 control circuit 23) for receiving instructions from the processor, the Auxiliary Processing Unit (APU) interface determining whether a given instruction is to be processed by the coprocessor (col 5 lines 53-59).

As per claim 3, Pereira discloses the method of claim 2, wherein the Auxiliary Processing Unit (APU) interface determining whether a given instruction is to be processed by the coprocessor includes the Auxiliary Processing Unit (APU) interface issuing a faulty commit if the given instruction is to be processed by the coprocessor

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and the field programmable gate array (FPGA) in the coprocessor is not programmed to perform a function corresponding to the given instruction (Col. 5 lines 53-59).

8. As per claim 4, Pereira discloses the method of claim 3, further comprising:

The processor initiating an exception subroutine responsive to the Auxiliary Processing Unit (APU) interface issuing a faulty commit; and (Col. 6 lines 1-3)

The exception routine identifying the configuration bit stream associated with the function for the application (Col. 6 lines 1-3) *The examiner asserts that "stalling the processor" and processing a separate task (loading the new configuration file) constitutes executing an exception subroutine.*

9. As per claim 5, Pereira discloses the method of claim 4, wherein the processor initiating an exception subroutine comprises:

The processor branching to the exception subroutine in response to the faulty commit. (Col. 6 lines 1-3) *The examiner asserts that Pereira's processor inherently branches to the subroutine for loading the new configuration file if the subroutine is to be executed.*

10. As per claim 6, Pereira discloses the method of claim 4, wherein the exception routine identifying the configuration bit stream comprises:

The exception routine decoding a function identifier; *The examiner asserts that a function must inherently be identified to the subroutine if the correct configuration file is to be fetched and loaded.*

The processor fetching the configuration bit stream associated with the function from a memory; (Col. 5 lines 53-57) and

The processor sending the configuration bit stream associated with the function corresponding to the given instruction to a direct memory access (DMA) channel coupled to the coprocessor for programming the field programmable gate array (PFGA) in the coprocessor (Col. 5 lines 53-57).

11. As per claim 7, Pereira discloses the method of claim 1, wherein dynamically programming the field programmable gate array (FPGA) comprises:

the processor performing a sequence of load and store instructions in accordance with an exception subroutine of the processor to program the field programmable gate array (FPGA) in accordance with the configuration bit stream. *The examiner asserts that with a limited number of bit-lines dedicated to programming the FPGA (Fig. 2 ports 20a,b and 22) and the "considerable overhead" required for loading a configuration file (Col. 2 lines 6-7), Pereira's processor must inherently perform multiple store instructions to transfer the data of the configuration file into the reconfigurable logic.*

12. As per claim 8, Pereira discloses the method of claim 1, further comprising:

The processor reissuing the instruction to the coprocessor responsive to the field programmable gate array (FPGA) being dynamically reconfigured to perform the function for the application. *The examiner asserts that after the reconfigurable logic has been reconfigured, the instruction is re-issued to the newly configured logic. (Col. 5 lines 59-60)*

13. As per claim 9, Pereira discloses a method for dynamically programming a field programmable gate array (FPGA) in a coprocessor (Fig. 1 reconfigurable logic 18 and col. 1 lines 28-29), the method comprising:

Providing a processor and a coprocessor that is separate from the processor, the coprocessor being coupled to the processor and including a field programmable gate array (FPGA) in the and an Auxiliary Processing Unit (APU) interface (see claim 1)

executing of an application using the processor; (Col. 4 lines 54-57)

the coprocessor receiving an instruction from the processor to perform a function for the application; (Col. 5 lines 45-49)

the Auxiliary Processing Unit (APU) interface issuing a faulty commit when the field programmable gate array (FPGA) in the coprocessor is not programmed to perform the function; (Col. 5 lines 53-59)

the processor initiating an exception subroutine in response to the faulty commit; (Col. 6 lines 1-3)



the exception subroutine fetching a configuration bit stream associated with the function for the application; (Col. 6 lines 1-3) *The examiner asserts that "stalling the processor" and processing a separate task (loading the new configuration file) constitutes executing an exception subroutine.*

The exception subroutine performing a sequence of load and store instructions to program the field programmable gate array (FPGA) in accordance with the configuration bit stream to perform the function. *The examiner asserts that with a limited number of bit-lines dedicated to programming the FPGA (Fig. 2 ports 20a,b and 22) and the "considerable overhead" required for loading a configuration file (Col. 2 lines 6-7), Pereira's processor must inherently perform multiple store instructions to transfer the data of the configuration file into the reconfigurable logic.*

14. As per claim 10, Pereira has taught a computer readable medium including instructions performing the method of claim 1, consequently claim 10 is rejected for the same reasons set forth in the rejection of claim 1 above.

15. As per claim 11, Pereira has taught a computer readable medium including instructions performing the method of claim 2, consequently claim 11 is rejected for the same reasons set forth in the rejection of claim 2 above.

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16. As per claim 12, Pereira has taught a computer readable medium including instructions performing the method of claim 3, consequently claim 12 is rejected for the same reasons set forth in the rejection of claim 3 above.

17. As per claim 13, Pereira has taught a computer readable medium including instructions performing the method of claim 4, consequently claim 13 is rejected for the same reasons set forth in the rejection of claim 4 above.

18. As per claim 14, Pereira has taught a computer readable medium including instructions performing the method of claim 5, consequently claim 14 is rejected for the same reasons set forth in the rejection of claim 5 above.

19. As per claim 15, Pereira has taught a computer readable medium including instructions performing the method of claim 6, consequently claim 15 is rejected for the same reasons set forth in the rejection of claim 6 above.

20. As per claim 16, Pereira has taught a computer readable medium including instructions performing the method of claim 7, consequently claim 16 is rejected for the same reasons set forth in the rejection of claim 7 above.

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21. As per claim 17, Pereira has taught a computer readable medium including instructions performing the method of claim 8, consequently claim 17 is rejected for the same reasons set forth in the rejection of claim 8 above.

22. As per claim 18, Pereira has taught a computer readable medium including instructions performing the method of claim 9, consequently claim 18 is rejected for the same reasons set forth in the rejection of claim 9 above.

### ***Response to Arguments***

1. Applicant's arguments filed May 22<sup>nd</sup>, 2006 have been fully considered but they are not persuasive.

2. Applicant states:

*"Applicant respectfully submits that that the title is descriptive of the invention."*

Examiner agrees. Objection has been withdrawn.

3. Applicant states:

*"Pereira, however, fails to disclose providing a coprocessor that is separate from the processor, in which the coprocessor is coupled to the processor and includes a field programmable gate array (FPGA), as recited in claim 1. Instead, Pereira discloses only providing a processor that includes a configurable functional unit (see FIG. 1). Pereira fails to disclose a coprocessor coupled to the processor, or a coprocessor that includes a field programmable gate array (FPGA). Claim 1 is, therefore, allowable over Pereira."*

Examiner disagrees. Applicant appears to believe that the language of claim 1 requires limitations that, as seen be Examiner, do not exist. Fig. 1 shows a

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Configurable FU 18 that is considered to be a coprocessor. The remainder of the logic shown in fig 1 is considered to be a portion of the processor—note in particular that reference 18 is not considered to be part of the processor in this office action. In that respect, the coprocessor is, in fact, separate from the processor. Regarding the remaining limitations, the coprocessor 18 is coupled to the processor (as shown in fig. 1) and does include a field programmable gate array. Examiner encourages Applicant to elaborate upon the intended meaning of the phrase “separate from the processor” within claim 1.

### ***Conclusion***


1. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire **THREE MONTHS** from the mailing date of this action. In the event a first reply is filed within **TWO MONTHS** of the mailing date of this final action and the advisory action is not mailed until after the end of the **THREE-MONTH** shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than **SIX MONTHS** from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Brian P. Johnson whose telephone number is (571) 272-2678. The examiner can normally be reached on 8-4:30 M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (571) 272-4162. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

  
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